PATENT COOPERATION TREATY

PCT

REC'D	18	APR 2006
WIPO		PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference N006P01-WO	FOR FURTHER ACT	FOR FURTHER ACTION See Form PCT/IPEA/416				
International application No.	International filing date (da	ay/month/year)	Priority date (day/month/year) 27.02.2004			
PCT/TR2004/000013 27.02.2004			27.02.2004			
International Patent Classification (IPC) or national classification and IPC INV. G06J1/00						
Applicant SARYAL, Nuri						
This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.						
2. This REPORT consists of						
3. This report is also accomp	anied by ANNEXES, comprising	;				
a. 🗌 sent to the applicar	nt and to the International Burea	u) a total of sheets, as	s follows:			
sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).						
sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.						
b. (sent to the International Bureau only) a total of (indicate type and number of electronic carrier(s)), containing a sequence listing and/or tables related thereto, in celectronic form only, as indicated in the Supplemental Box						
sequence listing and/or tables related thereto, in delectionic form only, as indicated in the Supplemental 2000. Relating to Sequence Listing (see Section 802 of the Administrative Instructions).						
4. This report contains indica	ations relating to the following ite	ems:				
☑ Box No. I Basis of	☐ Box No. I Basis of the report					
☐ Box No. II Priority						
☐ Box No. III Non-est	ablishment of opinion with regar	d to novelty, inventive	step and industrial applicability			
☐ Box No. IV Lack of	unity of invention	at the section of the				
applical	Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement					
☐ Box No. VI Certain documents cited						
☐ Box No. VII Certain defects in the international applic						
☐ Box No. VIII Certain	observations on the international	al application				
Date of submission of the demand		Date of completion of th	is report			
21.09.2005		18.04.2006				
Name and mailing address of the international		Authorized officer				
preliminary examining authority: ———————————————————————————————————	fice - P.B. 5818 Patentlaan 2		: 1 m			
NL-2280 HV Rijswiji	k - Pavs Bas	Filip, L	Parting Officer			
Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016		Telephone No. +31 70 3	340-			
1		1				

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No. PCT/TR2004/000013

-	Day No. 1 Davis (1)			
-	Box No. I Basis of the rep			
1	 With regard to the language, this report is based on the international application in the language in which it w filed, unless otherwise indicated under this item. 			
	international search (in publication of the internation of the interna	ranslations from the original language into the following language , a translation furnished for the purposes of: under Rules 12.3 and 23.1(b)) rnational application (under Rule 12.4) ary examination (under Rules 55.2 and/or 55.3)		
2	 With regard to the elements* have been furnished to the re 	of the international application, this report is based on (replacement sheets which ceiving Office in response to an invitation under Article 14 are referred to in this are not annexed to this report):		
	Description, Pages			
	1-12	as originally filed		
	Claims, Numbers			
	1-14	as originally filed		
	Drawings, Sheets			
	1/12-12/12	as originally filed		
	☐ a sequence listing and/or a	any related table(s) - see Supplemental Box Relating to Sequence Listing		
3.	 □ The amendments have resulted in the cancellation of: □ the description, pages □ the claims, Nos. □ the drawings, sheets/figs □ the sequence listing (specify): □ any table(s) related to sequence listing (specify): 			
1.	☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)). ☐ the description, pages ☐ the claims, Nos. ☐ the drawings, sheets/figs ☐ the sequence listing (specify): ☐ any table(s) related to sequence listing (specify):			
	* If item 4 applies, s	ome or all of these sheets may be marked "superseded."		

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No. PCT/TR2004/000013

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)

Yes: Claims

1-14

No: Claims

No:

Inventive step (IS)

Yes: Claims

Claims

1-14

Industrial applicability (IA)

Yes: Claims

1-14

No: Claims

2. Citations and explanations (Rule 70.7):

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:

D1: EP 0308583 A (AUTOMATION SYSTEMS 29-03-1989)

D2: US 6316992 B1 (DELANO CARY L ET AL 13-11-2001)

 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 1 does not involve an inventive step in the sense of Article 33(3) PCT.

D1 discloses:

A hybrid computer comprising at least one cell having at least one integrator circuit in which time dependent input voltage is applied through at least one input resistance and its sign is changed after the integration (Fig. 8), at least one cell having at least one analog integrator circuit in which the input voltage is applied to the inverting input of Opamp to change sign, then applied to at least one resistor (Fig. 6 e), at least one cell having at least one coordinator circuit (Fig. 7) and at least one analog integrator circuit connected to said coordinator circuit (implied, depending on configuration and external commands different output circuits, see Fig. 4, column 8, lines 19-22, 43-46, and column 13 lines 41-47), a micro controller (Fig. 1 - "CONTROLLER LOGIC 300", column 16, lines 5-12) and a digital computer (implied, column 16, lines 5-12 - "...programable controller...") including a data acquisition system (Fig. 1 - "DIGITAL SENSORS 201", "ANALOG SENSORS 12"), said hybrid computer characterized in that;

- Analog integrator circuits interconnected over coordinator circuits that perform synchronized and time continuous integration (implied).
- Data transferring from analog circuits to digital computer at desired intervals and displaying the results after processing (implied, column 16, lines 2-4).

The subject-matter of claim 1 therefore differs from D1 in that correcting the errors caused by the drift voltage is done by:

- Disconnection of all analog integrators from each other at required time intervals, loading of the magnified error voltage that occurs when the input voltage of the Opamp's is set to zero, in the memory included in the integrator circuits;
- As the analog integrator circuits are interconnected again, demagnifying the error voltages that are loaded in the memories, by the same ratio of magnification applied during

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (SEPARATE SHEET)

International application No.

PCT/TR2004/000013

loading and use it to eliminate error during integration.

The problem to be solved by the present invention may therefore be regarded as how to dynamically and automatically correct the errors caused by the drift voltage in the analog circuits.

The skilled person is aware that D2 addresses the voltage error correction by alternatively disconnecting all analog integrators at periodical time intervals, loading of the magnified error voltage that occurs when the input voltage of the Opamp's is set to zero, in the memory and as the analog integrator circuits are interconnected again, demagnifying the error voltages that are loaded in the memories, by the same ratio of magnification applied during loading (column 4, lines 23-47), and that would solve the above mentioned problem.

 Dependent claims 2-14 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of inventive step, see documents D1, D2 and the corresponding passages cited in the search report.